CLAIMS

1. A semiconductor integrated circuit device comprising:

a semiconductor substrate on which a plurality of transistors including gate insulation films of different thicknesses are formed; and

an input/output terminal formed on the semiconductor substrate, a transistor connected directly to the input/output terminal being one of the transistors other than a transistor having the thinnest gate insulation film.

2. A semiconductor integrated circuit device according to claim 1, further comprising a power supply terminal to which an external power supply voltage is applied, wherein a transistor connected directly to the power supply terminal ~~being~~ is one of the transistors other than the transistor having the thinnest gate insulation film.

3. A semiconductor integrated circuit device according to claim 1, further comprising a power supply terminal to which an external power supply voltage is applied and a ground terminal, a transistor whose current path is connected between the power supply terminal and the ground terminal being one of the transistors other than the transistor having the thinnest gate insulation film.

4. A semiconductor integrated circuit device according to claim 1, further comprising an interface

circuit connected to the input/output terminal, a transistor which constitutes part of the interface circuit and is connected directly to the input/output terminal being one of the transistors other than the transistor having the thinnest gate insulation film.

5. A semiconductor integrated circuit device according to claim 4, wherein a transistor which constitutes part of the interface circuit and is connected directly to a power supply terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

6. A semiconductor integrated circuit device according to claim 5, wherein a transistor ~~which constitutes part of the interface circuit~~ the interface circuit included in and having a current path connected between the power supply terminal and a ground terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

7. A semiconductor integrated circuit device according to claim 4, wherein said interface circuit includes an input buffer circuit.

8. A semiconductor integrated circuit device according to claim 4, wherein said interface circuit includes an output buffer circuit.

9. A semiconductor integrated circuit device according to claim 4, wherein said interface circuit includes a level shifter and an output buffer circuit.

10. A semiconductor integrated circuit device according to claim 1, further comprising a regulator circuit, a transistor which constitutes part of the regulator circuit and is connected directly to the power supply terminal being one of the transistors other than the transistor having the thinnest gate insulation film.

11. A semiconductor integrated circuit device according to claim 10, wherein a transistor which constitutes part of the regulator circuit having a current path connected between the power supply terminal and a ground terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

12. A semiconductor integrated circuit device according to claim 1, further comprising a regulator circuit, a transistor which is connected directly to an output node of the regulator circuit is the transistor having the thinnest gate insulation film.

13. A semiconductor integrated circuit device according to claim 9, further comprising a regulator circuit, said level shifter converting a lowered potential level signal obtained from the regulator circuit into a power supply voltage level signal to be supplied to an external terminal.

14. A semiconductor integrated circuit device according to claim 13, wherein a transistor which

constitutes part of the level shifter and is included in a device directly receiving the lowered potential level signal is the transistor having the thinnest gate insulation film.

15. A semiconductor integrated circuit device according to claim 1, further comprising a sensing circuit, connected to the input/output terminal, for sensing a third high level voltage input which is higher than an external power supply voltage, a transistor which constitutes part of the sensing circuit and is connected directly to the input/output terminal being one of the transistors other than the transistor having the thinnest gate insulation film.

16. A semiconductor integrated circuit device according to claim 15, wherein a transistor which constitutes part of the sensing circuit and is connected directly to a power supply terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

17. A flash EEPROM (electrically erasable programmable read-only memory) comprising:

a memory cell array formed on a semiconductor substrate; and

a control circuit, formed on the semiconductor substrate and connected to a plurality of memory cells that constitute the memory cell array, for controlling nodes of the memory cells, said control circuit

including a Y-selector whose gate is applied with an internally boosted voltage at a time of reading.

18. A flash EEPROM according to claim 17, wherein a plurality of transistors including gate insulation films of different thicknesses are formed on the semiconductor substrate, and said Y-selector is formed of a transistor which is other than a transistor having the thinnest gate insulation film.

19. A flash EEPROM (electrically erasable programmable read-only memory) comprising:

a memory cell array formed on a semiconductor substrate; and

a control circuit, formed on the semiconductor substrate and connected to a plurality of memory cells that constitute the memory cell array, for controlling nodes of the memory cells, said control circuit including a source decoder whose NMOS driver gate is applied with an internally boosted voltage at a time of reading.

20. A flash EEPROM according to claim 19, wherein a plurality of transistors including gate insulation films of different thicknesses are formed on the semiconductor substrate, and said source decoder is formed of a transistor which is other than a transistor having the thinnest gate insulation film.

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